SITe® SI03xA 24 µm Charge-Coupled Device Family

The SITe® SI03xA family of 24 µm Charge-Coupled Device (CCD) image sensors are full-frame, 100% fill-factor devices intended for use in moderate-resolution scientific, commercial, and industrial applications where high dynamic range, broad spectral sensitivity, high quantum efficiency, and low noise are required. These applications include:

- Inspections
- Spectroscopy
- Astronomy
- Photo Calorimetry
- Optical Measurements
- BioMedical Research
- Mammography
- Bone Densitometry
- DNA Testing
- Aerospace
- Protein Crystallography

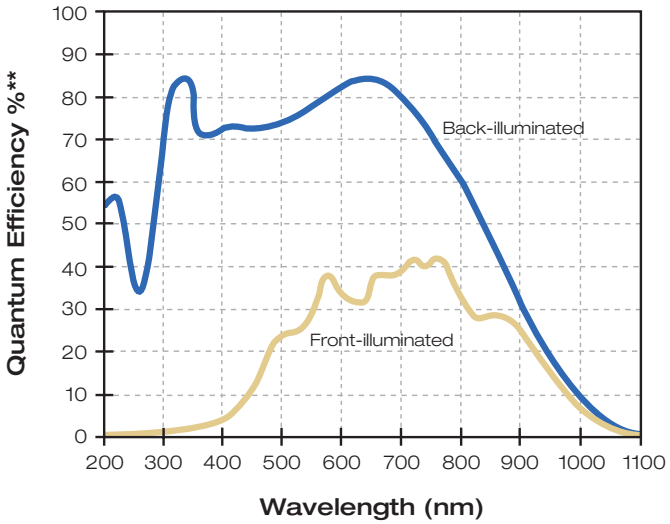
The SI03xA family includes both front-illuminated (SI032AF and SI033AF) and thinned, back-illuminated (SI032AB and SI033AB) versions. Both device types have a series-parallel-series architecture with square pixels, 24 µm on a side.

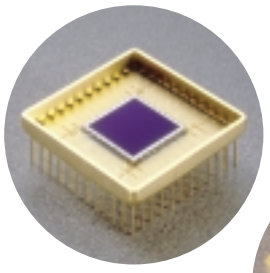
Multi-pinned phase (MPP*) mode operation is available in the SI03xA family. This allows the user to take advantage of the inherently low dark current that can be achieved (2 to 10 pA/cm^2 at 20C). For many applications this means a thermoelectric cooler may be used instead of more complex cooling systems, reducing size, weight, and cost of the imaging system.

Under normal operating conditions the SI03xA family has an output sensitivity of approximately 2.6 µV/e$^-$ and a typical noise of 5e$^-$ rms at 50k pixels/second data rate. The full well is nominally 350,000 electrons. Coupled with the noise of 5e$^-$, this provides a dynamic range of 70,000, more than a full 16 bits.

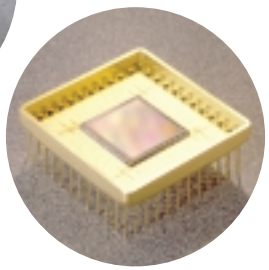
The SI032A has an imaging area (parallel array) consisting of 512 vertical columns with 512 pixels in each column. The upper and lower edges of the parallel array are each bounded by a horizontal (serial) register, one end of which is terminated in an output structure, providing two possible outputs. The device can be operated to read the entire array out either output. The details of these arrangements are provided in the functional description section.

**MPP, multi-pinned phase, is a patented technology.*
***QE based on typical data.*

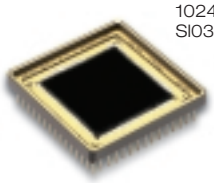




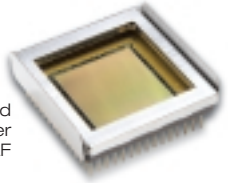
512 x 512 Back-illuminated
SI032AB



512 x 512 Front-illuminated
SI032AF



1024 x 1024 Back-illuminated
SI033AB



1024 x 1024 Front-illuminated
with protective cover
SI033AF

SITe 512 x 512 Back SI032B 24 micron imager	SITe 512 x 512 Front SI032F 24 micron imager	SITe 1024 x 1024 Back SI033B 24 micron imager	SITe 1024 x 1024 Front SI033F 24 micron imager
FEATURES	**FEATURES**	**FEATURES**	**FEATURES**
Moderate speed readout <1MHz	Moderate speed readout <2 MHz	Moderate speed readout <1MHz	Moderate speed readout <2 MHz
Large dynamic range and low noise	Large dynamic range and low noise	Large dynamic range and low noise	Large dynamic range and low noise
High sensitivity	High sensitivity	High sensitivity	High sensitivity
High visible QE	Moderate visible QE	High visible QE	Moderate visible QE
Uniform response	Uniform response	Uniform response	Uniform response
Response from soft X-ray to short IR	Response from 400 nm to short IR	Response from soft X-ray to short IR	Response from 400 nm to short IR
Medium format area	Medium format area	Large format area	Large format area
Medium resolution	Medium resolution	Medium resolution	Medium resolution
One or two outputs*	One or two outputs*	One, two, or four outputs	One, two, or four outputs
Full frame imager	Full frame imager	Full frame imager	Full frame imager

**Image cannot be read out two outputs simultaneously.*

The SI033A has an imaging area (parallel array) consisting of 1024 vertical columns with 1024 pixels in each column. The upper and lower edges of the parallel array are each bounded by a horizontal (serial) register, each end of which is terminated in an output structure, providing four potential outputs. The device is structured such that four distinct output configurations can be implemented: four outputs, one per quadrant, two outputs, one per half, split vertically or horizontally, or one output for the entire device. The facility for multiple outputs operating simultaneously increases the maximum possible frame rate by a factor of two or four over that of a single output. The details of these arrangements are provided in the functional description section.

SI03xA Functional Description

The parallel section of the SI032A consists of an orthogonal array of 512 x 512 picture elements (pixels). The array consists of 512 optically separate columns each of which contains 512 pixels.

The SI033A is an array of 1024 x 1024 pixels. It is divided into an upper and lower half at row 512. Each half can be independently clocked such that the upper and lower halves can be read out through their respective serial registers. Alternatively, the whole array can be read out through one serial register.

Each pixel consists of three polysilicon gates, referred to as phases P1, P2, and P3. Pixels in each column electrically share the same three poly electrodes. Each pixel is both an optical sensing site where the photoelectrically generated signal charge can be collected, as well as a holding site for integrated signal charge. The quantity of charge is linearly proportional to the local intensity of the light falling on the chip and the integration time. The pixel electrodes are sequentially clocked to move that charge toward the serial register for subsequent readout.

An additional column exists on each side of the imaging array to collect dark current and optically-generated charges that are created in the region outside of the array. This excess charge is collected by the reset drain and does not enter the serial register.

The transfer gate is the last gate in the array prior to shifting the charge packets into the serial readout register. The gate is logically a P3 gate and may be clocked with the P3 electrodes.

The serial register is oriented orthogonally to the columns in the parallel section. Each pixel in the serial register is aligned with a column in the parallel section. A row of pixels from the parallel section is transferred, in parallel, into the serial register. The charge packets are then transferred along the serial register to the output amplifier for sensing and conversion to an electrical signal. Each serial pixel can contain approximately 3 times the capacity of a parallel pixel.

There are 16 extended pixels in the serial register between the first pixel in the array and the output amplifier. These extra pixels can be used to determine the system offset.

The summing well is used to noiselessly sum charge packets on-chip prior to being read out.

The last gate separates the summing well from the output amplifier and isolates the output node from the serial clocks.

The output consists of a floating diffusion amplifier using a single stage source follower. The source diode of the reset transistor is the floating diffusion onto which charge from the serial register is transferred. The gate of the MOSFET is connected directly to the floating diffusion. When charge is transferred to the floating diffusion the resulting voltage change is reflected in a change in the current through the MOSFET and its external load resistor of 3 to 50 kΩ.

Multi-pinned phase (MPP) operating mode, supported by all members of the SI03xA family, significantly reduces background dark current for longer integration time and/or higher operating temperatures.

The SI03xAB is thinned to approximately 13 µm and illuminated from the back surface. The back-illuminated mode of operation allows much higher quantum efficiency to be achieved and extends the useful spectral range from 0.1 nm in the soft x-ray to 1100 nm in the near IR. Such thinned devices are rugged, fully supported, and flat to ±10 µm or less across the imaging surface.

The SI032A and SI033A functional diagrams, timing diagrams and pinout lists are available for inspection and download at www.site-inc.com.

SI03xA Operating Characteristics

DC Voltages

Function	*Pin*	*Min*	*Typical*	*Max*	*Unit*
Output drain supply	VDDx	22	25	28	V
Reset drain	RDx	12	15	17	V
Last gate	LGx	-5	-4	0	V
Package	SUB		0		V
Input diode (SI032A only)	IDx	5	15	25	V
Chip ground	GNDx		0		V
Output load	OUTx	3	20	50	kOhm

x = output A, B, C or D

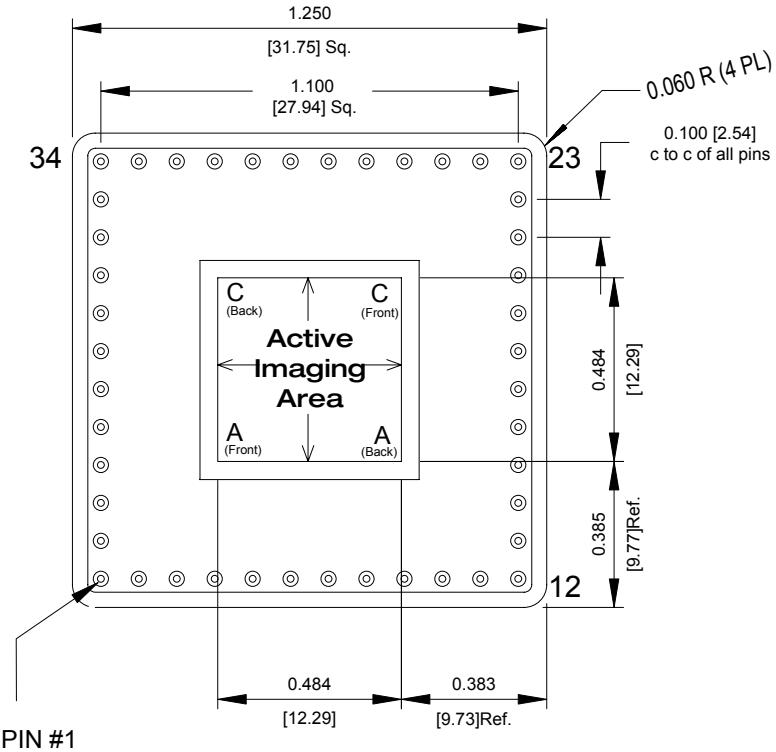
Clock Voltages

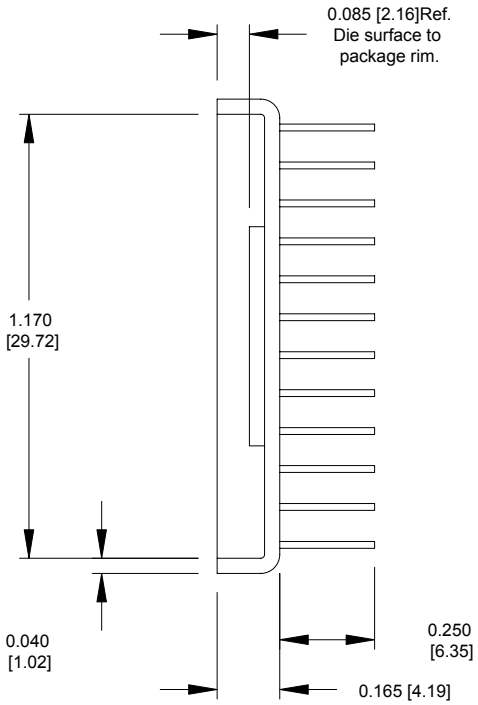
Function	*Pin*		*Min*	*Typical*	*Max*	*Unit*
Reset gate	RGx	Low rail	-5	0	5	V
		High rail	5	12	15	V
Serial clocks	S#x	Low rail	-10	-6	0	V
		High rail	5	6	15	V
Parallel clocks	P#x	Low rail	-10	-9	0	V
	P1x, P2x	High rail	0	4	10	V
	P3x	High rail	0	2	10	V
Summing well	SWx	Low rail	-10	-6	0	V
		High rail	5	6	15	V
Transfer gate	TGx	Low rail	-10	-9	0	V
		High rail	0	2	10	V
Sample gate (SI032A only)	SGx	Low rail	-10	-6	0	V
		High rail	5	6	15	V

x = output A, B, C or D

Note: It is recommended that the maximum peak-to-peak voltage between any two neighboring gates not exceed 20V.

SI032A 44 Lead Kovar Package



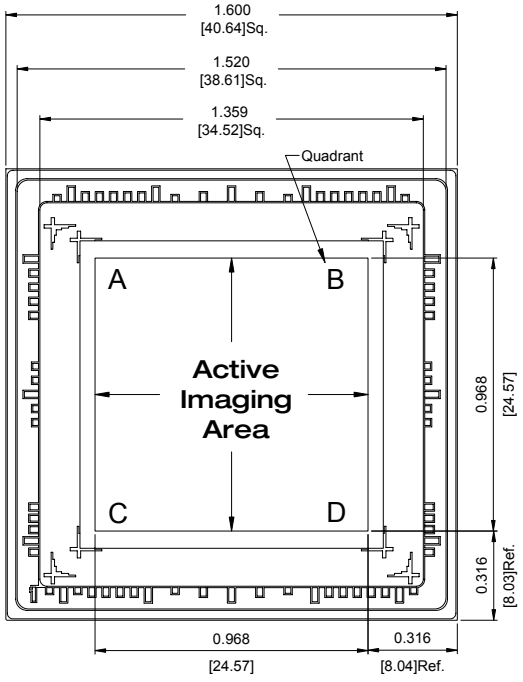


PIN #1
Identified by uniquely colored glass bead
(other pins use same colored glass beads).

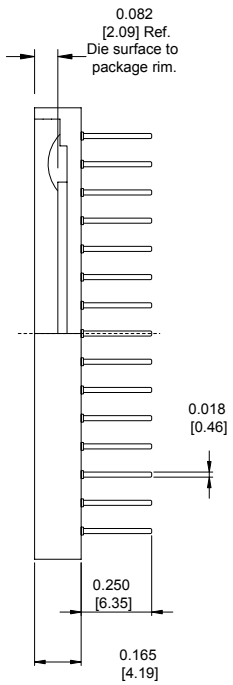
Units are in
inches [mm]

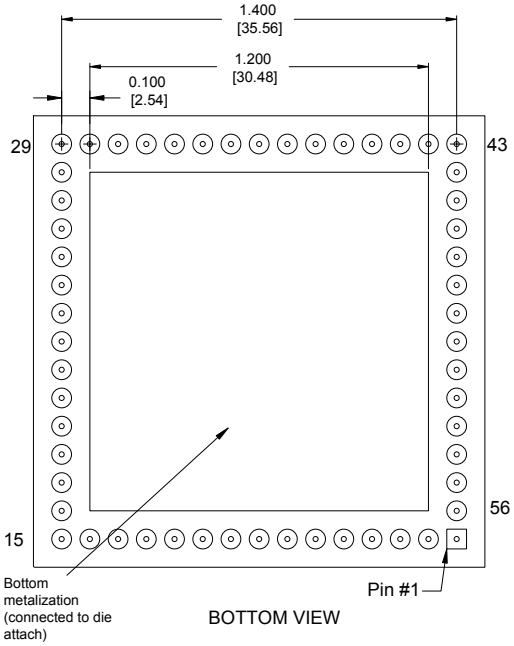
49-032-M-02 Rev. 02
01/07/03

SI033A 56 Lead Ceramic Package



Units are in Inches [mm]





BOTTOM VIEW

49-033-M-01 Rev 02
01/07/03

SI03xA Performance Specifications

Parameter			*Minimum*	*Typical*	*Maximum*	*Comment*
Format	SI032A			512 x 512		pixels
	SI033A			1024 x 1024		pixels
Pixel size				24 x 24		µm
Imaging area	SI032A			12.3 x 12.3		mm
	SI033A			24.6 x 24.6		mm
Fill factor				100		%
Dark current (MPP)			2	10	50	pA/cm^2 (1)
Sensitivity	SI032A		2.5	2.8	3.1	$\mu V/e^-$
	SI033A		2.1	2.4	2.7	$\mu V/e^-$
Noise	Front		3.5	5	7	rms e^-
	Back		4	7	9	rms e^-
Well capacity			300,000	350,000		e^- (2)
CTE	Serial		0.99995	0.99999		
	Parallel		0.99995	0.99999		
Clocking frequency	SI032A	Front		0.5	<2.0	MHz
		Back		0.5	<1.0	MHz
	SI033A	Front		0.5	<2.0	MHz
		Back		0.5	<1.0	MHz
Capacitance	SI032A	Parallel		7500		pF (3)
		Serial		13		pF (4)
	SI033A	Parallel		15000		pF (5)
		Serial		31		pF (4)
Flatness	SI032A	Front			±10	µm
		Back			±10	µm
	SI033A	Front			±10	µm
		Back			±10	µm

1 Dark current measured at -15C and extrapolated to 20C.
2 Well capacity measured by photon transfer technique.
3 Capacitance/phase for entire array.
4 Capacitance/phase for entire serial register.
5 Capacitance/phase for 512 x 1024 pixels.

SI03xA Ordering Options & Information

To order a member of the SI03xA family, per standard configuration, options must be specified in the following format:

SI03xA	C	-G	O

Step 1–Basic part number

SI03xA
x=2 (SI032A)
x=3 (SI033A)

Step 2–Insert configuration

F=Front-illuminated
B=Back-illuminated

Step 3–Insert grade as specified in the Defects chart at right

1=Grade 1
2=Grade 2 (SI033A Only)
ENG=Engineering grade*

**Engineering grade CCDs are guaranteed to provide imaging functionality only; no defect specification is guaranteed.*

Step 4–Number of functional outputs

SI032
1=1 Guaranteed output amplifier
2=2 Guaranteed output amplifiers

SI033
1=1 Guaranteed output amplifier
2=2 Guaranteed output amplifiers
4=4 Guaranteed output amplifiers

Defects

	Grade 1 Max Allowed Defects		*Grade 2 Max Allowed Defects*
Applicable to	SI032A	SI033A	SI033
Pixels	10	40	80
Clusters	*	6	12
Adjacent clusters	*	3	6
Columns	0	0	4

**Individual defects within clusters are included in the total pixel defect specification.*

For example, a front illuminated grade 1, dual output SI032A device is ordered as an SI032AF-12, and a back-illuminated engineering grade SI033A device is ordered as an SI033AB-ENG1. Engineering grade units may be specified only with a single output; grade 2 devices may be specified with a maximum of 2 outputs.

If you have special or custom requirements not encompassed by SI032A and SI033A standard configurations, please contact SITe Customer Service for custom ordering instructions. All custom requirements must be submitted in writing to SITe Customer Service in order to receive proper attention.

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REV 4/03 S002